REMARKS

Claims 1-16 are pending.

Claims 1-16 stand rejected.

Claims 7 is objected to.

Claim 2, 12-13 are cancelled.

Claim 4, 5, 7, 9, 10, 11, 14, 15 and 16 are currently amended.

Claims Rejections Based on 35 U.S.C. § 102

The examiner has rejected claims 1, and 3-9 as being anticipated by Campanini U.S. Patent No. 4,700,292 (Campanini or '292).

As support for its argument that the present invention is anticipated under 35 USC 102 the examiner cites Campanini "...locations are identified by the contents of register MEA read out into bus OB; the arrival of each writing command WR at signal receiver RIS (FIG. 4), which immediately precedes each incoming data word, causes the incrementation of the contents of register MEA and the decrementation of the numerical value stored in word counter WCA substantially concurrently with similar operations in the interface of the master processor" (col. 9, lines 26-34). The present invention attempts to solve a problem similar to Campanini, but each invention utilizes a different solution. Because the solutions are different the parts of the respective systems are different. In fact the present invention has no component that provides for a decrementation of the numerical value stored in a word counter. Conversely, Campanini neither discloses nor suggests: a control register that does not contain any word count, but nonetheless achieves the transfer of data from one memory to another. In '292, the WCA accepts information that includes a numerical value, which represents the total number of data words to be transferred (Col. 7, lines 20). The control register of the current disclosure does not require a numerical value representative of the total number of data words to be transferred, because transfer is accomplished by setting a starting address and writing to memory in a block dependent upon the number of accesses made to the coprocessor. Furthermore the WCA stores the number of words to be transferred and then decrements the word count upon the transfer of

each word. The control register in the current invention does not decrement any count, because it need not know the count, since memory accesses and corresponding write signals move the data into contiguous memory locations.

Furthermore, there is no equivalent MEA in the present invention. The 292 MEA represents an address register that is loaded with the address of the cells of the working memory. Afterwards the MEA is incremented for each memory data transfer, serving to set the memory location for the next transfer. The current invention, by contrast begins with a pointer and increments the pointer every time there is access by the co processor. A pointer increments from a base point, but is not an address in and of itself. The memory pointer adjusts upon each write signal's rising edge. Campanini writes a starting address and a word count and then counts the words, while incrementing memory. The present disclosure simply responds to the co processor's access. Campanini does not anticipate the present invention, because its WCA and MEA perform functions distinct from the control register of the present invention.

The examiner asserts that "a data register having a data register system address" is anticipated by '292 in regards to the REI register because the "...data register receives all incoming words where the words are then propagated to the buffer store (FIFO) and ultimately, to the appropriate destination within the internal memory (See, OA, para. b3)." The REI does not perform the same function as the present invention's data register 123 nor does it have any functional or structural similarity. The REI is located inside the line control unit. The start of procedure word representing the *number of data words* to be transferred, arrives at register REI which generates CDC (FIG. 2). CDC is a code corrector (the present disclosure utilizes no code correction), and then CDC, among other things, transfers *number of data words* through gate A1 to the WCA. As previously indicated the '292 WCA stores the number of words to be transferred and then decrements the word count upon the transfer of each word. The present invention control register does not decrement any count.

Additionally, the data register 123 does not *store the number of words to be transferred and does not decrement any number thereafter,* but receives a word of data on data bus 144 and writes that word into the internal memory location of memory 125 as specified by signals generated by chip select and internal address generator unit 122. The function of the REI by itself or in conjunction with WCA does not perform the same function or encompass the same structure of the data register 123.

Regarding the assertion that the present invention does not have a buffer store that stores FIFO, the data in the present invention is stored in memory blocks directly, and is essentially dynamic so that as data comes to the bus from the coprocessor, the data is stored.

The examiner points to the fact that Campanini utilizes the "...arrival of each writing command WR at signal receiver RIS (FIG. 4), which *immediately precedes* each incoming data word, causes the incrementation of the contents of register MEA and the decrementation of the numerical value stored in word counter ..", as indicative of the '292 WR signal acting as a system address for the data register. Firstly, characterizing the REI, MEA or WCA as data registers is inappropriate in that they are counters. Putting aside such a characterization, in the present invention, the WRN signal 134 selects a bank in memory, which receives the data word provided on the data bus 144. In the present invention the WRN signal triggers the internal address generator to select consecutive memory locations on the internal memory. For a write operation, for example, the WRN signal 134 permits a write to the selected memory bank, of the word appearing on local or internal data bus 136, which receives the data word provided on external data bus 144 during the bus cycle following the control word (pg. 5, lines 15-18).

The examiner indicates that the present invention's "internal address generator coupled to the control register and to the internal memory", is anticipated by Campanini because the "MEA control register initially holds the starting internal memory address. This address is incremented by an internal address generator each time a new word is being transferred to memory." The MEA seems to hold the entire address which it then increments. In the present invention, the internal address generator merely serves as a pointer to a memory location. Pointing to an address and the actual address are two different concepts. Furthermore, the pointer is moved each time the coprocessor is accessed. So long as address bus 142 asserts the data address for the data register 123, the co-processor continues to write subsequently received words from data bus 144 into consecutive locations of memory 125. The schema in Campanini requires that the MEA read out into the bus OB; the arrival of each writing command WR at signal receiver RIS (FIG. 4), which immediately precedes each incoming data word, causes the incrementation of the contents of register MEA and the decrementation of the numerical value stored in word counter WCA.

The examiner notes (OA, para.1c,) that when the first processor places a control word having a burst mode bit and a starting internal address on the data bus it asserts the control register system address on the system bus. This operational feature of the present invention is

compared to Campanini in that its word count is put in the WCA control register and the starting address is put in the MEA register. Clearly to write into a memory location an address is required, but in Campanini, as indicated, it uses the WCA and the MEA as counters that increment and decrement addresses and word counts. The only relation to the control register, is that it does contain an address, but not an address to be decremented. WCA and MEA have no functional relation to the control register in the present invention.

The examiner also notes (OA, para.1d), that the second processor enters a burst mode in which the internal address generator selects consecutive memory locations starting at the internal addressed specified by the control word in the control register. The examiner then notes that the word count, stored in the WCA register, includes a burst mode indication. The examiner, thus finds a burst mode in '292, where such does not exist. The inventors have chosen to define burst mode as incrementing the address without decrementing the word count and so long as address bus 142 asserts the data address for the data register 123, the co-processor will write subsequently received words from data bus 144 into consecutive locations of memory 125. The address specified is referred to as a "starting address," because it is the first or starting address of a contiguous section of memory into/from which a block of words is written/read during a burst data transfer. When processor 110 wishes to end the burst data transfer, it may, for example, assert the system address of some other control register, or of control register 121 and write all 0s into the control register. It is clear that no burst mode exists in Campanini, as that term is used in the present invention. Respectfully, the comparison drawn by the examiner is not appropriate to the subject of what burst means in the present invention.

Essentially, the points made by the examiner in paragraph 1e and 1f, are rebutted by showing that the present invention does not use the WCA to store the number of words to be transferred and then decrements the word count upon the transfer of each word. The control register 121 does not decrement any count. It need not know the count, because accesses and write signals move the data into memory.

To write either a single word of data or a block of data in burst mode, the processor 144 first strobes the CS line 141, and selects the control register 121 by placing its 11-bit system address on system address line 142 (e.g., address 370). The WRN line 143 is also strobed with a logic low signal. Thus, in a first bus cycle, a 16-bit control word is transferred via data bus 144 to 16-bit control register 121.

Nowhere in '292 does it teach that this control word specifies a unique (internal) address of memory 125 (15 bits total) as well as whether control register 121 implements an auto-increment (burst) mode. The address field of the control word comprises *two fields*: a 5-bit field which selects one of the 32 memory banks of memory 125; and a 10-bit field which specifies a unique memory address location within a given selected memory bank 125. Campanini, even if, it included a burst mode indication as defined by the examiner, does not teach that the present invention burst mode increments the address pointer without decrementing the word count. Nowhere in Campanini does it teach that so long as address bus 142 asserts the data address for the data register 123, co-processor will continue to write subsequently received words from data bus 144 into consecutive locations of memory 125. The MEA represents an address register that is loaded with the address of the cell of the working memory. Afterwards the MEA increments for each memory data transfer. Campanini and the present invention are quite distinct on this point of operation.

Regarding claim 3, Campanini neither discloses nor suggests that when processor 110 wishes to end the burst data transfer, it may, for example, assert the system address of some other control register, or of control register 121 and write all 0s into the control register. In fact only when there is no data left to transfer does the WR signal stop being asserted.

It is well recognized that to constitute an anticipation, all material elements recited in a claim must be found in one unit of prior art. For reasons indicated above, the present invention does not include *each and every element* of Campanini, which therefore precludes Campanini from being used as a reference against the present invention.

Claims 3, 6, 7, 8 and 9 depend upon an allowable independent claim 1 for the reasons stated and are therefore not subject to rejection. However, claim 4, 5, 7, 8 and 9, as had been presented in the Preliminary Amendment, have been amended to place the matter in a condition for allowance. In as much as the Applicant has cancelled claims 2, 12, and 13, the corresponding rejection must be withdrawn.

Applicant respectfully disagrees with and explicitly traverses the examiner's reasons for rejecting claim 1, and 3-9 as being anticipated by Campanini in view of the foregoing. The examiner is respectfully requested to reconsider and withdraw the rejection.

Rejections Based on 35 U.S.C. 103 (a)

Claim 2 and 10-16 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Campanini. Claim 2 has been cancelled.

As amended claims 10, 11, 14, 15 and 16 no longer refer to an integrated circuit, since the invention is an apparatus that is not limited by its implementation. In its amended form Claim 10 is now drawn more properly to a multiprocessor system.

A claimed invention is *prima facie* obvious when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference or combined references must teach or suggest all the claim limitations.

Generally, as regards claims 10, 11, 14, 15 and 16, each in its amended form, makes no reference to an integrated circuit. As such, Campanini does not teach or suggest all the claim limitations. Furthermore, claims 11, 14, 15 and 16 depend from claim 10, and therefore must be allowed based upon an allowable base claim. In further support of claims 10, 11, 14, 15 and 16, Campanini does not shows the overall combination claimed in the present invention and more specifically those elements now embodied in claim 10.

As regards to rejections, under 35 U.S.C. 103 of claims 10, 11, 14, 15 and 16 on the grounds of the reference cited, contrary to the examiner's position, Campanini does not teach, disclose, or provide the motivation for one skilled in the art to develop the features of the present invention as suggested by the examiner.

Claims 11, 14-16 depend upon an allowable independent claim 10 for the reasons stated and are therefore not subject to rejection. However, claim 10, 11, 14-16, as had been presented in the Preliminary Amendment, have been amended to place the matter in a condition for allowance. In as much as the Applicant has cancelled Claim 12 and 13, the corresponding rejection must be withdrawn.

Applicant respectfully disagrees with, and explicitly traverses, the examiner's reasons for rejecting claim 10, 11, 14,15 and 16 as being obvious in view of Campanini and accordingly the examiner is respectfully requested to reconsider and withdraw the rejection.

Support for the amendments

Amendments to claim 5, pg. 3, lines 11-15 and lines 18-20; claim 7, pg. 3, lines 6-8; claim 8, pg. 3, lines 18-20; claim 9, pg. 5, lines 6-7; claim 10-15, lines 14-16 and lines 17-20. No new matter has been added. Claim 7 has been amended in accordance with the examiner's suggestion so as to remove objection.

Conclusion

Having addressed the examiner's rejections under 35 USC § 102 (b), and 35 USC § 103, applicant submits that the reasons for the examiner's rejections have been overcome and can no longer be sustained. Applicant respectfully requests reconsideration and withdrawal of the rejections and that a Notice of Allowance be issued. Please inform the applicant, through his attorney, if the examiner differs in that view. Should any unresolved issues remain, the examiner is invited to call Applicant's attorney at 212-692-1052. The Commissioner for Patents is hereby authorized to charge any additional fees, including fees for extensions of time or credit any excess payment that may be associated with this communication to Duane Morris LLP deposit account 50-2061.

Respectfully submitted,
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